

REMARKS

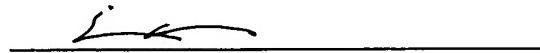
The Official Action mailed February 16, 2006, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on March 19, 2002; July 15, 2004; December 20, 2004; May 9, 2005; and November 29, 2005. A further Information Disclosure Statement was filed on March 28, 2006 (received by OIPE March 30, 2006), and consideration of that Information Disclosure Statement is respectfully requested.

Claims 7-14, 21-29 and 37-55 were pending in the present application prior to the above amendment. The Applicant notes with appreciation the allowance of claims 7-14, 21, 22, 24, 25 and 37-46 (page 3, Paper No. 10099972). Paragraphs 2 and 3 of the Official Action reject claims 23, 26-29 and 47-55 as obvious based on the combination of U.S. Patent No. 6,440,865 to Lee, Wolf et al., *Silicon Processing for the VLSI Era, Volume 1 – Process Technology*, page 518, and U.S. Patent No. 5,747,361 to Ouellet, either alone or in combination with U.S. Patent No. 5,912,506 to Colgan. In response, claims 23, 26-29 and 47-55 have been canceled without prejudice or disclaimer. Accordingly, claims 7-14, 21, 22, 24, 25 and 37-46 are now pending in the present application, of which claims 7-10, 21, 22, 24, 25 and 37-40 are independent, and all of which are believed to be in condition for allowance.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,


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